WHAT IS CLAIMED IS:

1. For use in an operational circuit having a high impedance node, a test circuit capable of connecting said high-impedance node to an external test point when a test signal driving said test circuit is enabled, said test circuit comprising:

a first transmission gate switch for coupling said high impedance node to a first internal node of said test circuit when said test signal is enabled, said first transmission gate switch comprising a first N-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said first internal node;

a second transmission gate switch capable of coupling said first internal node to a second internal node of said test circuit when said test signal is enabled;

a third transmission gate switch capable of coupling said second internal node to said external test point when said test signal is enabled; and

a biasing circuit for generating a negative Vgs bias on said first N-channel transistor when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor.

2. The test circuit as set forth in Claim 1 wherein said first transmission gate switch comprises a first P-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said first internal node.

3. The test circuit as set forth in Claim 2 wherein said biasing circuit generates a positive Vgs bias on said first P-channel transistor when said test signal is disabled to thereby reduce leakage current in said first P-channel transistor.

4. The test circuit as set forth in Claim 3 wherein said biasing circuit comprises a first impedance circuit coupled between said first internal node and a VDD power supply rail and a second impedance circuit coupled between said first internal node and a ground rail, wherein said first and second impedance circuits form a voltage divider circuit that biases said first internal node to a target bias voltage when said test signal is disabled.

5. The test circuit as set forth in Claim 4 wherein said gate of said first N-channel transistor is coupled to a Logic 0 when said test signal is disabled and said biasing circuit biases said target bias voltage on said first internal node coupled to said source of said first N-channel transistor to a voltage greater than Logic 0 to thereby generate said negative Vgs bias on said first N-channel transistor.

6. The test circuit as set forth in Claim 5 wherein said gate of said first P-channel transistor is coupled to a Logic 1 when said test signal is disabled and said biasing circuit biases said target bias voltage on said first internal node coupled to said source of said first P-channel transistor to a voltage less than Logic 1 to thereby generate said positive Vgs bias on said first P-channel transistor.

7. The test circuit as set forth in Claim 6 wherein said second transmission gate switch comprises a second N-channel transistor having a drain coupled to said first internal node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said second internal node.

8. The test circuit as set forth in Claim 7 wherein said second transmission gate switch comprises a second P-channel transistor having a drain coupled to said first internal node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said second internal node.

9. The test circuit as set forth in Claim 8 wherein said third transmission gate switch comprises a third N-channel transistor having a drain coupled to said second internal node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said external test point.

10. The test circuit as set forth in Claim 9 wherein said third transmission gate switch comprises a third P-channel transistor having a drain coupled to said second internal node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said external test point.

11. A signal generator comprising a phase-locked loop (PLL) circuit capable of generating an output reference signal having a desired frequency, said PLL circuit comprising:

a voltage-controlled oscillator;

a charge pump and loop filter circuit for generating a control voltage capable of controlling said voltage controlled oscillator; and

a test circuit capable of connecting a high-impedance node of said PLL circuit to an external test point when a test signal driving said test circuit is enabled, said test circuit comprising:

a first transmission gate switch for coupling said high impedance node to a first internal node of said test circuit when said test signal is enabled, said first transmission gate switch comprising a first N-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said first internal node;

a second transmission gate switch capable of coupling said first internal node to a second internal node of said test circuit when said test signal is enabled;

a third transmission gate switch capable of coupling said second internal node to said external test point when

said test signal is enabled; and

a biasing circuit for generating a negative Vgs bias on said first N-channel transistor when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor.

12. The signal generator as set forth in Claim 11 wherein said first transmission gate switch comprises a first P-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said first internal node.

13. The signal generator as set forth in Claim 12 wherein said biasing circuit generates a positive Vgs bias on said first P-channel transistor when said test signal is disabled to thereby reduce leakage current in said first P-channel transistor.

14. The signal generator as set forth in Claim 13 wherein said biasing circuit comprises a first impedance circuit coupled between said first internal node and a VDD power supply rail and a second impedance circuit coupled between said first internal node and a ground rail, wherein said first and second impedance circuits form a voltage divider circuit that biases said first internal node to a target bias voltage when said test signal is disabled.

15. The signal generator as set forth in Claim 14 wherein said gate of said first N-channel transistor is coupled to a Logic 0 when said test signal is disabled and said biasing circuit biases said target bias voltage on said first internal node coupled to said source of said first N-channel transistor to a voltage greater than Logic 0 to thereby generate said negative Vgs bias on said first N-channel transistor.

16. The signal generator as set forth in Claim 15 wherein said gate of said first P-channel transistor is coupled to a Logic 1 when said test signal is disabled and said biasing circuit biases said target bias voltage on said first internal node coupled to said source of said first P-channel transistor to a voltage less than Logic 1 to thereby generate said positive Vgs bias on said first P-channel transistor.

17. The signal generator as set forth in Claim 16 wherein said second transmission gate switch comprises a second N-channel transistor having a drain coupled to said first internal node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said second internal node.

18. The signal generator as set forth in Claim 17 wherein said second transmission gate switch comprises a second P-channel transistor having a drain coupled to said first internal node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said second internal node.

19. The signal generator as set forth in Claim 18 wherein said third transmission gate switch comprises a third N-channel transistor having a drain coupled to said second internal node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said external test point.

20. The signal generator as set forth in Claim 19 wherein said third transmission gate switch comprises a third P-channel transistor having a drain coupled to said second internal node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said external test point.